IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No	10/431,822
Priority Filing Date	May 8, 2003
Inventor	Terry Gilton et al.
Assignee	Micron Technology, Inc.
Priority Group Art Unit	2812
Priority Examiner	Walter L. Lindsay Jr.
Attorney Docket No	MI22-2462
Customer No	021567
Title Methods of Forming Electronic Con	nponents, and a Conductive Line

INFORMATION DISCLOSURE STATEMENT PURSUANT TO 37 C.F.R. §§ 1.56, 1.97 AND 1.98

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a continuation application of co-pending application Serial No. 10/431,822, filed May 8, 2003. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. § 1.98(d) and MPEP § 609(2).

Citation of these references is respectfully requested.

Respectfully submitted,

Dated: (2-15-03

Mark S. Matkin

Mark S. Matkin Reg. No. 32,268

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

ATTY. DOCKET NO. MI22-2462

PRIORITY SERIAL NO. 10/431,822

LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)

APPLICANT: Terry Gilton et al.

PRIORITY FILING DATE March 8, 2003

PRIORITY GROUP ART UNIT 2812

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*Examiner's Initials		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
_	AA	4,599,118	07/1986	Han et al.		·	
	AB	4,786,609	11/1988	Chen			
	AC	4,954,867	09/1990	Hosaka			
	AD	4,971,655	11/1990	Stefano			
	AE	4,981,810	01/1991	Fazan et al.		;	
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	АН	5,219,777	06/1993	Kang			
	Al	5,252,352	11/1993	Woo et al.		•	-

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			Date	Country	Class	Subclass	Yes	No
	2	58-25265	05/1983	Japan (Imai)				
	AK	62-90974	09/1987	Japan (Kawamura)				
	AL	64-73772	03/1989	Japan (Koyama)	•			

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	АМ		Wolf et al., SILICON PROCESSING FOR THE VLSI ERA, pp. 66-71 (1986).
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	AN		Wolf et al., SILICON PROCESSING FOR THE VLSI ERA, pp. 208 and 212 (1986).
-	AO		Wolf et al., SILICON PROCESSING FOR THE VLSI ERA, pp. 216-218 (1986).
EXAMINER			DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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	AA	5,28	6,344	02/1994	Blalock				0	
	AB	5,29	0,720	03/1994	Chen					
	AC	5,30	06,655	04/1994	Kurimoto					
	AD	5,30	06,951	04/1994	Lee et al.			-		
	AE	5,31	4,834	05/1994	Mazure et al.			• •	· ·	
	AF	5,32	22,807	06/1994	Chen et al.					,
	AG	5,33	34,556	08/1994	Guldi	•				ı.
	АН	5,37	1,026	12/1994	Hayden					
	Al	5,38	32,533	01/1995	Ahmad et al.					
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	AB	5,430,313	07/1995	Kumagai et al.			-		
	AC	5,439,846	08/1995	Nguyen et al.					
	AD	5,476,802	12/1995	Yamazaki					
	AE	5,491,100	02/1996	Lee et al.					
	AF	5,512,771	04/1996	Hiroki et al.				,	
	AG	5,545,578	08/1996	Park et al.					
	AH	5,552,329	09/1996	Kim et al.		_	•		
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	AB	5,668,028	09/1997	Bryant							
	AC	5,682,055	10/1997	Huang et al.					9		
	AD	5,714,413	02/1998	Brigham et al.					÷		
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	AG	5,798,279	08/1998	Crisenze et al.							
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	Al	5,994,192	11/1999	Chen					٠		
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	AB	6,040,241	03/2000	Lee et al.					
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